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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,903	09/26/2001	Yoshikazu Kasuya	15.48/6066	9431

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KONRAD RAYNES VICTOR & MANN, LLP
315 SOUTH BEVERLY DRIVE
SUITE 210
BEVERLY HILLS, CA 90212

EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/963,903	Applicant(s) KASUYA, YOSHIKAZU	
	Examiner Steven H. Rao	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *14-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file claiming priority from Japanese Patent Application No. 2000-292141 filed on September 26, 2000.

It is noted, however, that applicant has not filed a certified copy of the Japanese Patent Application No. 2000-29214 as required by 35 U.S.C. 119(b).

Election/Restrictions

Applicant's election without traverse of Group II, claims 1-13 in Paper No. 9 is acknowledged.

Double Patenting

Claims 1-13 of this application conflict with claims 1-11 of Application No. 09/963,903. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application.

Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claim s 1-13 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-11 of copending Application No. 09/963,903. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Drawings

The drawings filed on September 26, 2001 have been accepted.

Specification

The disclosure is objected to because of the following informalities: specification page 1 lines 5-12 applicants' refer to two co-pending U.S. applications that are related to this case by attorney docket numbers only, however as applications now have the serial numbers of these applications, they (the related applications) must be identified by their serial numbers also.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1-11 the phrase "conduction layer renders the claim indefinite because the term "conduction layer " is indefinite. If applicants' mean " conductive layer". It is suggested that all occurrences of " conduction layer " be replaced with " conductive layer".

In claim 2 line 3 the phrase, " the second insulation layer and the sidewall insulation layers are composed of a material that is more difficult to etch than the first insulation layer " it is not clear what applicants' intend to included/excluded by the phrase" is more difficult to etch".

Further the specification, prior art or knowledge of one of ordinary skill in the art cannot clarify or provide guidance as to applicants' intend to include/exclude by the above recitation.

In claim 4, lines 6-7, the phrase " wherein the first through hole is continuous to the second through hole "

it is not clear what applicants' intend to included/excluded by the phrase" wherein the first through hole is continuous to the second through hole ".

Further the specification, prior art or knowledge of one of ordinary skill in the art cannot clarify or provide guidance as to applicants' intend to include/exclude by the above recitation.

Appropriate correction is required.

In claims 10-11 the term, " ion implantation operation" is used. It is suggested that the word ' operation" be deleted.

Claim 11 is also rejected for failing to further limit from claim 10.

Claims 2-4 and 6-9 are rejected for at least depending directly or indirectly upon rejected claims 1 and 5.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 , 6,9 –13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misra et al. (U.S. Patent No. 5,960,270 herein after Misra, also cited by applicants' in their Ids).

With respect to claims 1 and 9, Misra describes a method of manufacturing a semiconductor device including the steps of : forming a gate dielectric layer on a semiconductor layer (fig. 10 # 105 on 102), forming a first conductive layer having a specified pattern on the gate dielectric layer (Fig. 11 # 108), forming sidewall spacers (insulation layers) on side walls of the first conductive layer (Fig. 12 # 114), forming a source region and a drain region in the semiconductor layer (fig. 12 # 118) depositing

first insulating layer covering the first conductive layer and the side wall spacers (Fig. 14 # 120) the first insulation layer comprising a material different from that of the sidewall insulation layers (105 oxide and ~~114~~ 120 nitride) , planarizing the first insulation layer until an upper surface of the first conduction layer is exposed (fig. 15, planarize 120 to expose 108) , removing a part of the first conduction layer in a manner so that the gate dielectric layer is not exposed to thereby form a recessed section on the first conduction layer between the insulating layers (fig. ~~16~~ 19, not exposing the gate oxide 125, col. 10 lines 1-16), to thereby from a recessed section on the conduction layer (fig. 19). It is noted that the figs. 19-22 show a second embodiment, however as stated in col. 10 lines 37-39, the steps describing the embodiment in figs. 10-16 are also used in the embodiment described in figs. 19-22 filling a second conduction layer in the recessed section to form a gate electrode that includes at least the first conduction layer and the second conduction layer. Forming a second insulation layer at the recessed section on the second conduction layer, the second insulation layer being composed of a material different from that of first insulation layer (Misra fig. 14 # 120 of nitride the first insulating layer of oxide), etching the first insulation layer to form a first through hole that reaches the source region or the drain region (Misra fig. 17, col. 18 lines 17-23), forming a first contact layer in the first through hole. (Misra fig. 17, # 128 a col. 18 lines 18).

With respect to claim 2, wherein in the step (j) , the second insulation layer and the sidewall insulation layer s are composed of a material that is more difficult to etch than the first insulation layer (Misra col. 10 lines 1-16, col. 6 lines 35-44)

a barrier layer is formed between the steps of removing a part of the first conduction layer and the step of filling the second conduction layer (Misra Fig. 20, col. 10 lines 39-40, photoresist layer , not shown in fig. 20).

With respect to claim 3, wherein the first conduction layer is formed from a material comprising silicon (Misra col. 9 line 31, layer 108 of polysilicon) and step h includes the steps of depositing a metal layer .for siliciding the first conduction layer , on the first conduction layer (Misra col. 10 lines 42-45), siliciding the first conduction layer to form a silicide layer (Misra col. 10 lines 57-60).

With respect to claim 4, to the extent understood, wherein the method step includes:

Forming a third insulation layer on the first insulation layer and the second insulation layer (Misra fig. 16 # 122, col. 9 line 57); etching the third insulation layer to form a second through hole (Misra fig. 20), forming a second contact layer in the second through hole, wherein the first through hole is continuous to the second through hole

wherein the second conductive layer is formed from a material selected from the group consisting of a metal, a metal alloy and a metal compound (Misra, col. 10 line 35).

With respect to claim 6, to the extent understood, wherein the first insulation layer comprises silicon oxide and the second insulation layer comprises silicon nitride . (Misra col. 9 line 26 and col. 9 lines 39-40).

With respect to claim 8, wherein the first insulation layer comprises silicon oxide and the sidewall insulation layers comprise silicon nitride . (Misra col. 9 line 26 and col. 9 lines 39-40).

With respect to claims 10 and 11, to the extent understood, repeat the steps of claims 1 and therefore are rejected for reasons set out under claim1 above.

With respect to claim 12, wherein the second conducting layer comprises a silicide (Misra col.9lines 49-50).

With respect to claim 13, wherein the removing a part of the first conduction layer further includes removing a greater depth of the first concentration layer from a center region rather than from end regions adjacent to the sidewall insulation layers . (Misra fig. 7 etc.)

Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misra et al. (U.S.Patent no. 5,960,270 herein after Misra, also cited by applicants' in their Ids) as applied to claims 1-4 above and further in view of Yamada et al. (U.S. Patent No. 6,465,359 herein after Yamada).

With respect to claim 5, wherein the method includes the second insulating layer being formed from a material having a ratio of an etching rate of the second insulating layer with respect to an etching rate of the first insulating layer being two or greater. ()

Misra as stated above discloses the second insulating layer as having a different etch rate as compared to the first insulating layer.

Misra does not specifically describe or state that the different etch rate has a ratio of two or greater.

However Yamada a patent from the same filed of endeavor, describes in col. 10 lines 25-30 etch ratio of Sio2 to SiNx to be 16.8 to provide an etching method which achieves a high selectivity ratio of oxide etch to etch of an etch stop.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Yamada's etch ratio in Misra's etching steps to provide an etching method which achieves a high selectivity ratio of oxide etch to etch of an etch stop. (Yamada col. 4 lines 29-33).

With respect to claim 7, after step (j) the sidewall insulation layers are formed from the first conductive material having an etching ration of the sidewall insulation layers with respect to an etching rate of the first insulation layer being two or greater. (Yamada col. 10 lines 25-30)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-3926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

SHR
10/29/02

Wael Fahmy
SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800